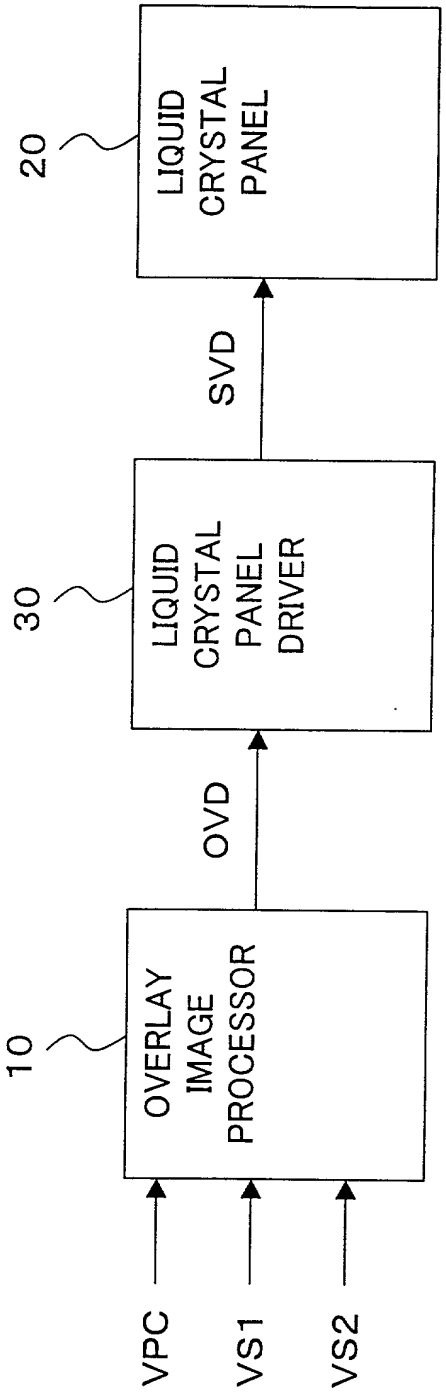

10
OVERLAY IMAGE PROCESSOR
OVD
30
LIQUID CRYSTAL PANEL DRIVER
SVD
20
LIQUID CRYSTAL PANEL
VPC
VS1
VS2

Fig. 1

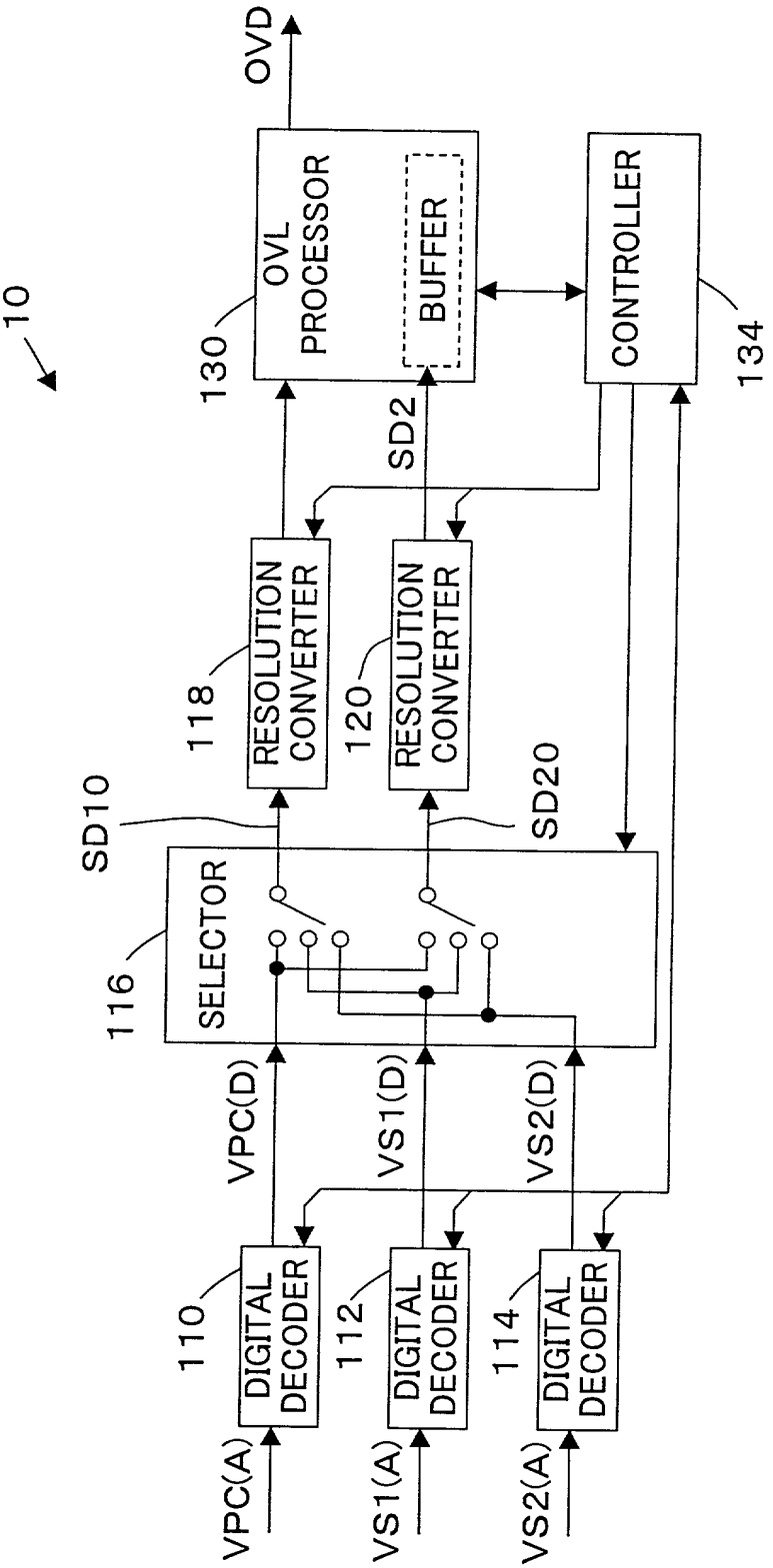
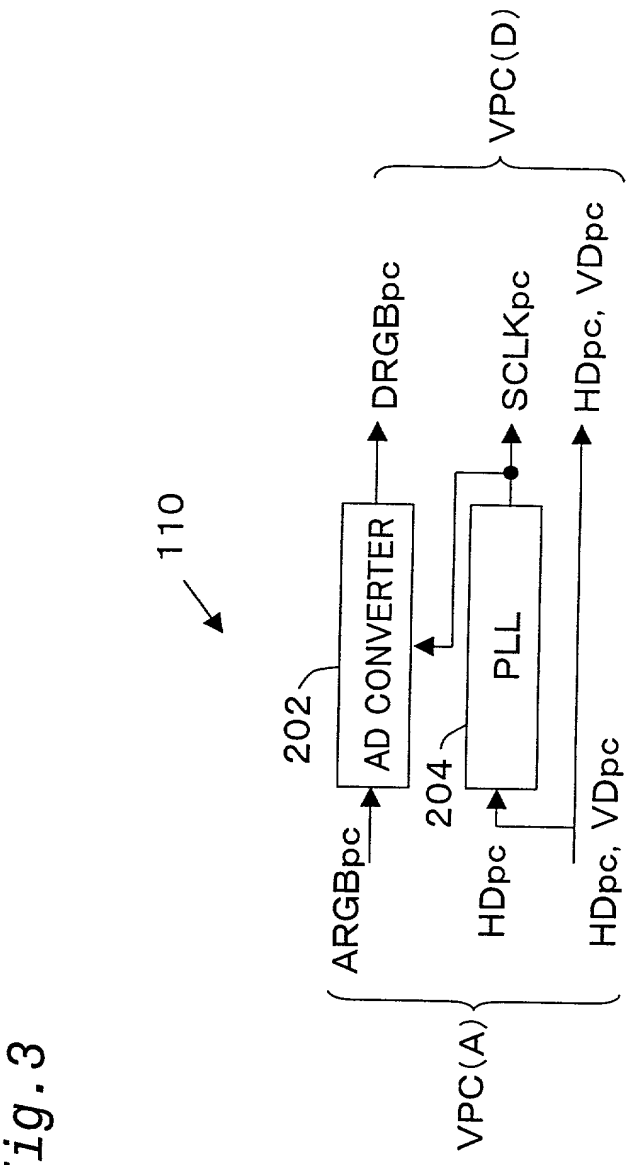

10
OVD
130
OVL PROCESSOR
BUFFER
CONTROLLER
134
SD2
118
RESOLUTION CONVERTER
120
RESOLUTION CONVERTER
SD10
SD20
116
SELECTOR
VPC(D)
VS1(D)
VS2(D)
110
DIGITAL DECODER
112
DIGITAL DECODER
114
DIGITAL DECODER
VPC(A)
VS1(A)
VS2(A)

Fig.2

Fig. 3


110
202
AD CONVERTER
204
PLL
ARGBpc
HDpc
DRGBpc
SCLKpc
HDpc, VDpc
HDpc, VDpc
VPC(A)
VPC(D)

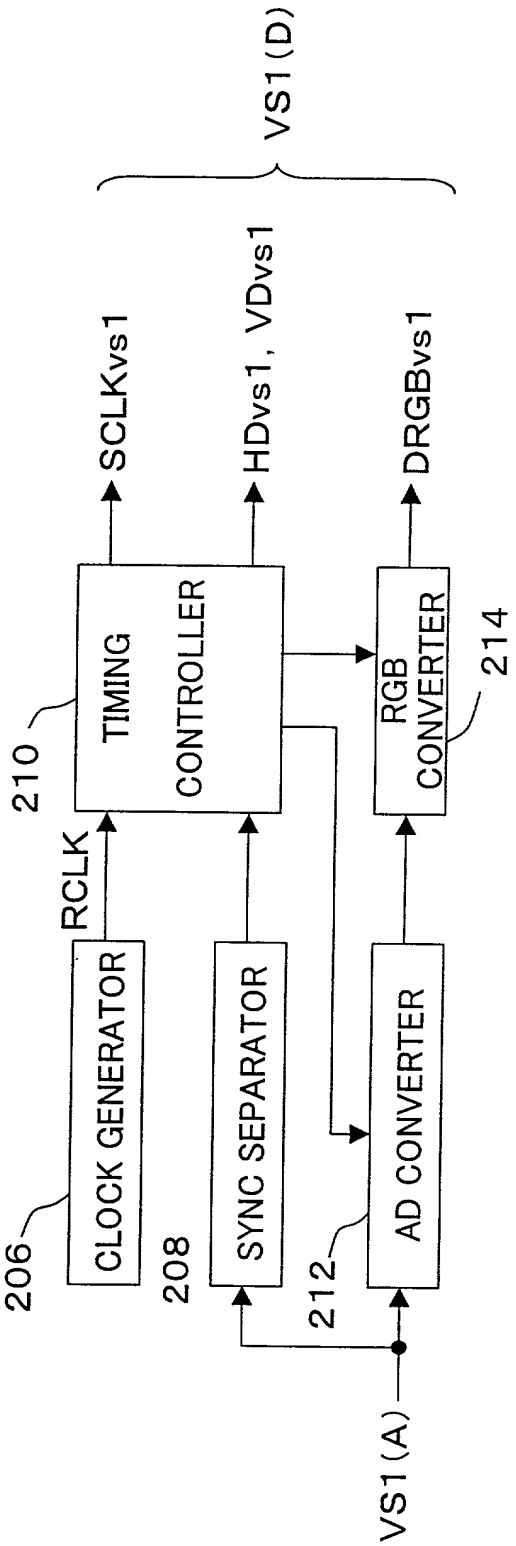

112
VS1 (D)
SCLKvs1
HDvs1, VDvs1
DRGBvs1
210
TIMING CONTROLLER
RGB CONVERTER
214
RCLK
206
CLOCK GENERATOR
208
SYNC SEPARATOR
212
AD CONVERTER
VS1 (A)

Fig. 4

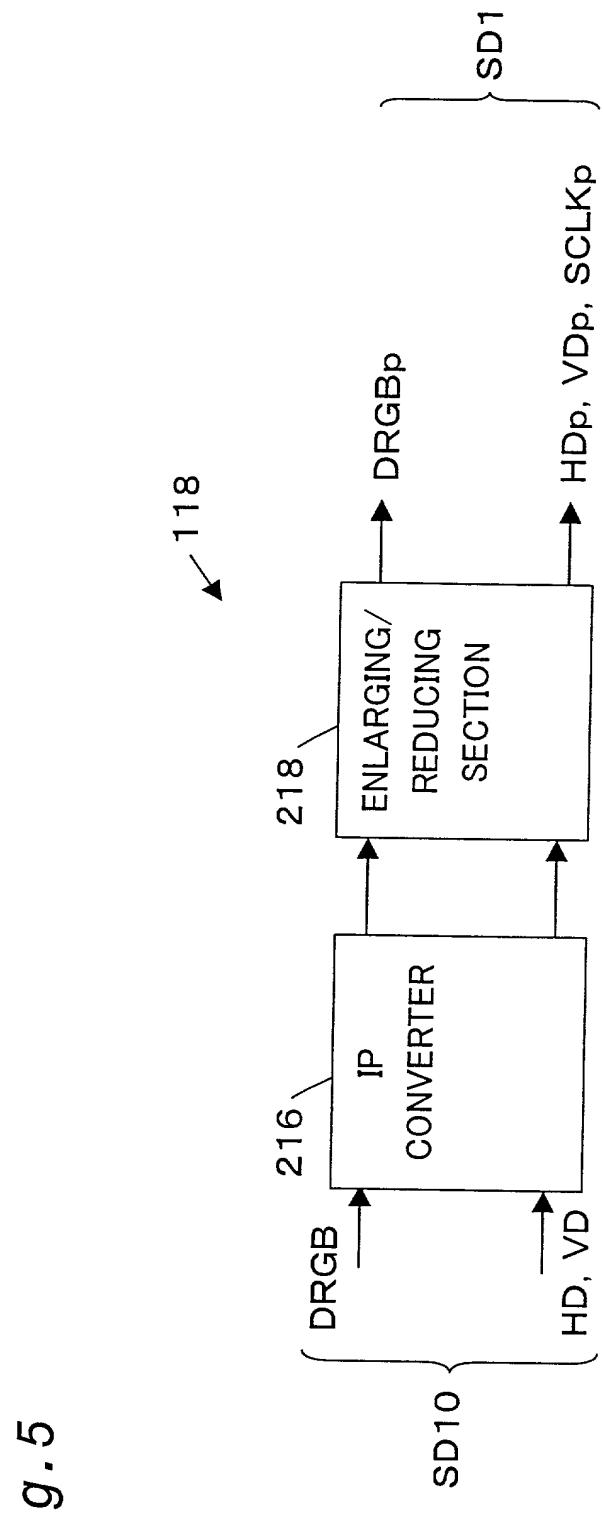

118
SD1
DRGBp
HDp, VDp, SCLKp
218
ENLARGING/
REDUCING
SECTION
216
IP
CONVERTER
DRGB
HD, VD
SD10

Fig. 5

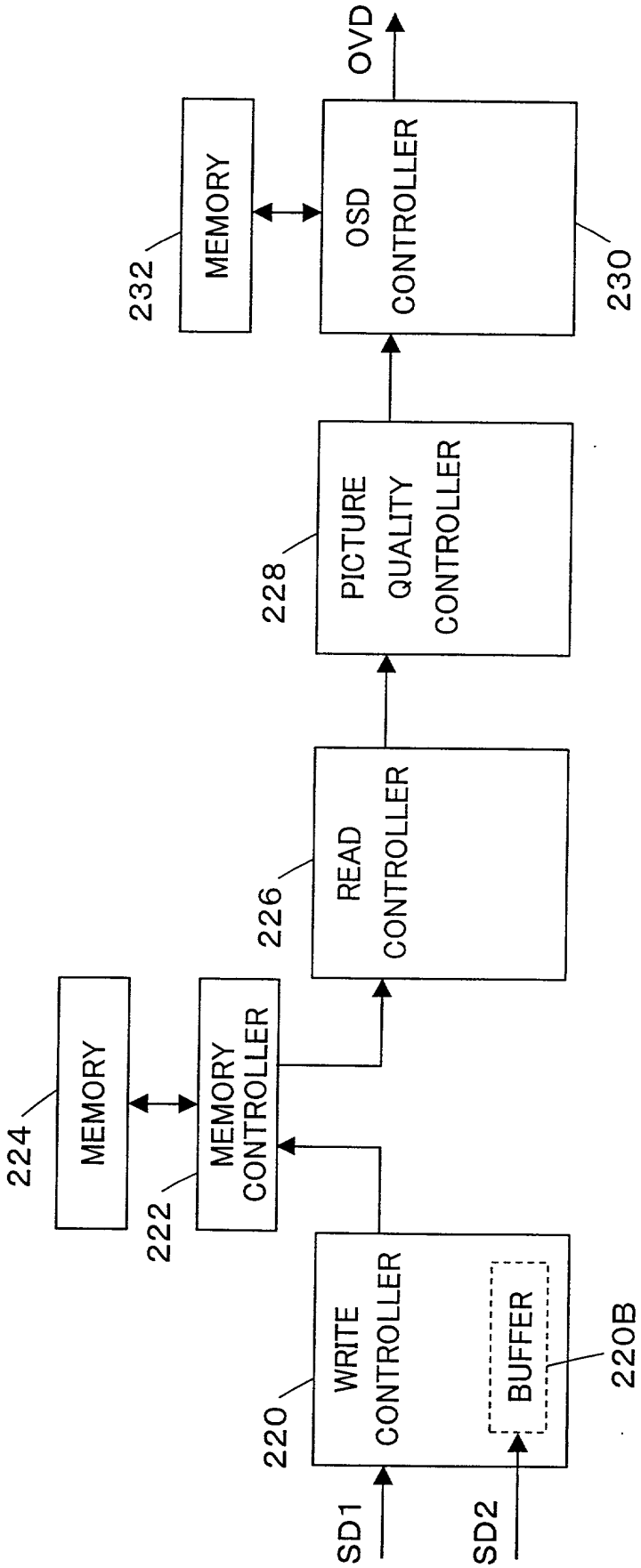

130
SD1
SD2
220
WRITE CONTROLLER
220B
BUFFER
222
MEMORY CONTROLLER
224
MEMORY
226
READ CONTROLLER
228
PICTURE QUALITY CONTROLLER
230
OSD CONTROLLER
232
MEMORY
OVD

Fig. 6

Fig.7(A)

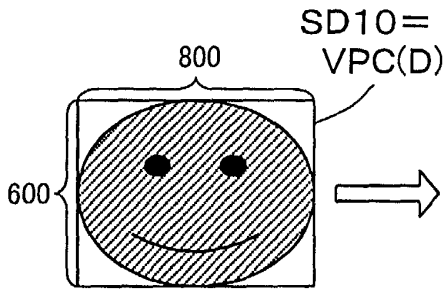


Fig.7(B)

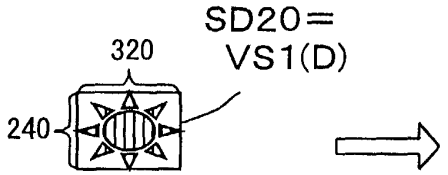


Fig.7(C)

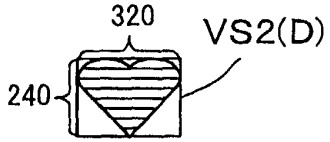


Fig.7(D)

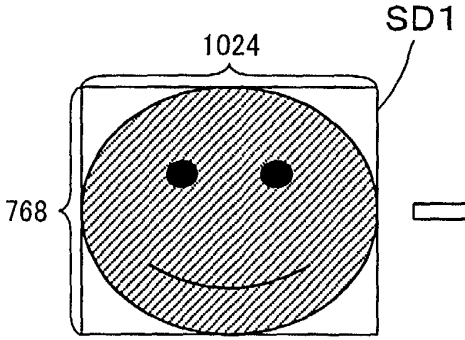


Fig.7(E)

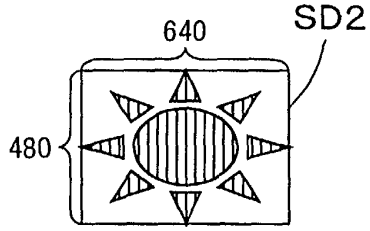


Fig.7(F)

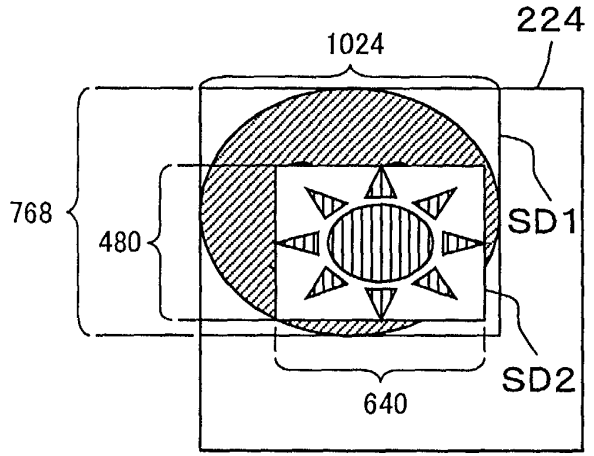


Fig. 8(A)

SD1:VPC, SD2:VS1

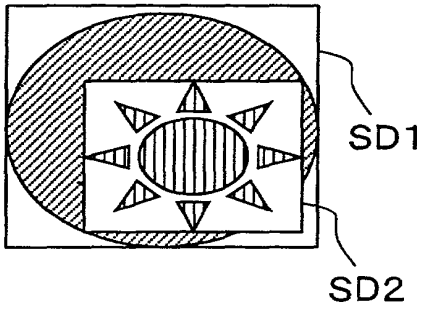


Fig. 8(B)

SD1:VPC, SD2:VS2

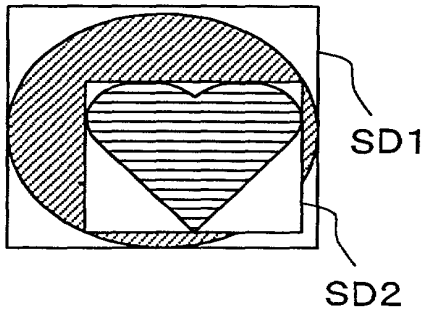


Fig. 8(C)

SD1:VS1, SD2:VS2

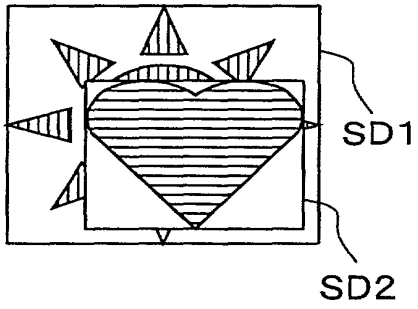


Fig. 8(D)

SD1:VS1, SD2:VPC

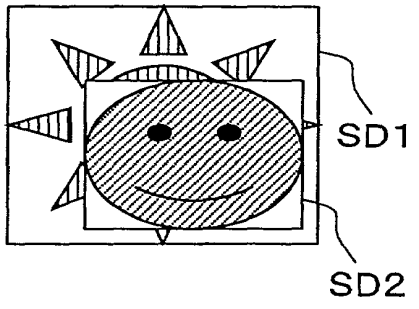


Fig. 8(E)

SD1:VS2, SD2:VS1

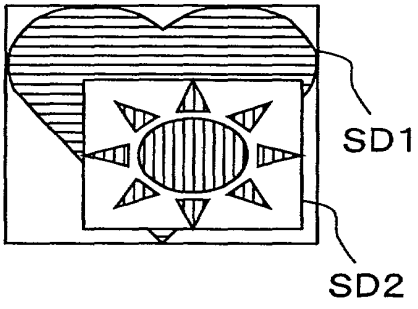
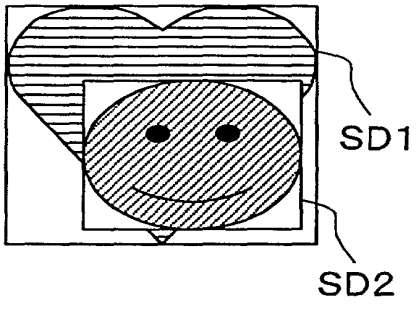


Fig. 8(F)

SD1:VS2, SD2:VPC



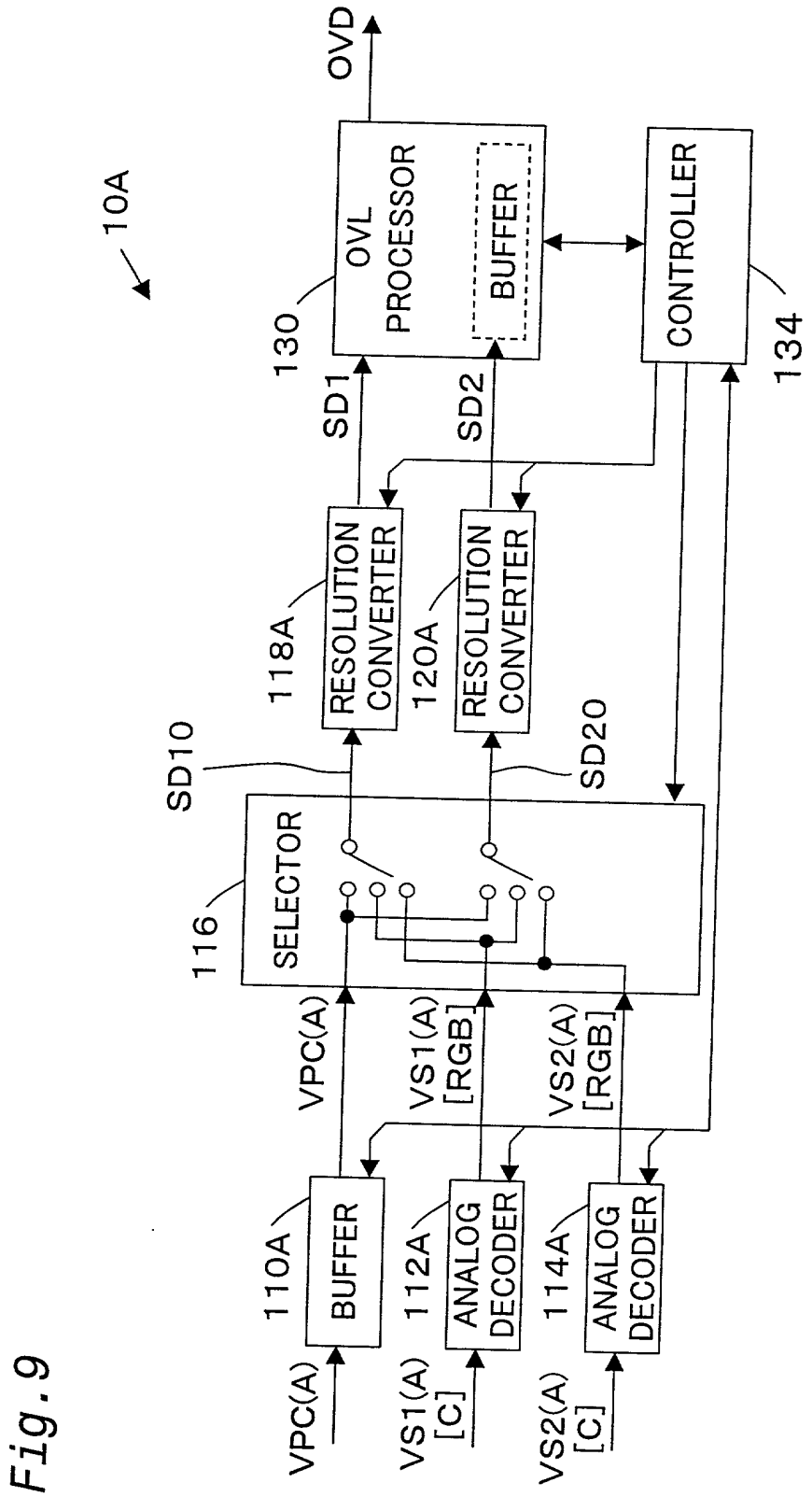

10A
OVD
130
OVL PROCESSOR
BUFFER
CONTROLLER
134
SD1
SD2
118A
RESOLUTION CONVERTER
120A
RESOLUTION CONVERTER
SD10
SD20
116
SELECTOR
VPC(A)
VS1(A) [RGB]
VS2(A) [RGB]
110A
BUFFER
112A
ANALOG DECODER
114A
ANALOG DECODER
VPC(A)
VS1(A) [C]
VS2(A) [C]

Fig. 9

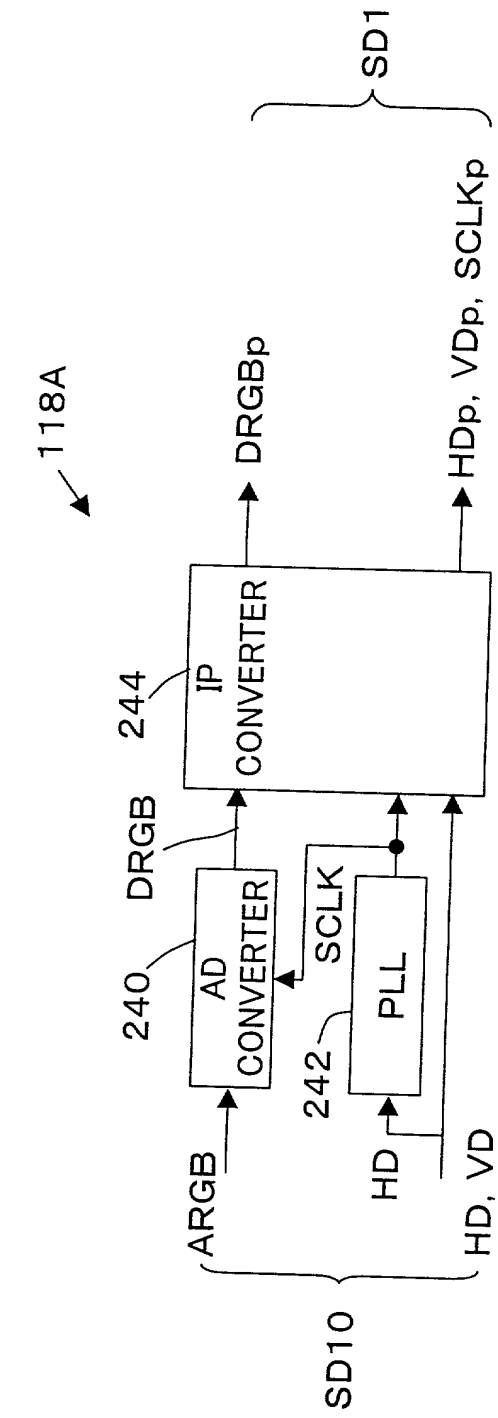

118A
SD1
DRGBp
HDp, VDp, SCLKp
244
IP CONVERTER
DRGB
240
AD CONVERTER
SCLK
242
PLL
ARGB
HD
HD, VD
SD10

Fig. 10

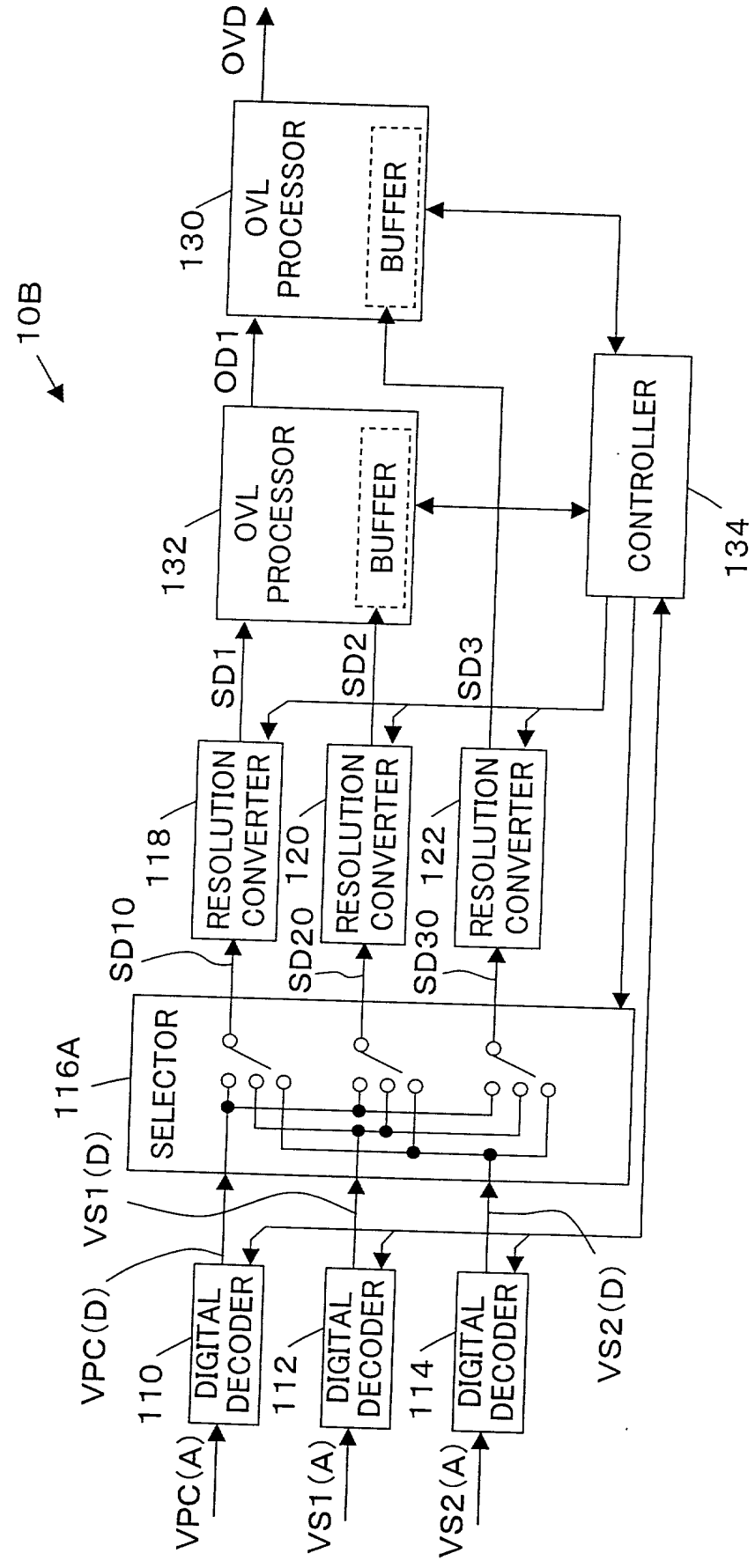

10B
OVD
130
OVL PROCESSOR
BUFFER
OD1
132
OVL PROCESSOR
BUFFER
CONTROLLER
134
SD1
SD2
SD3
118
RESOLUTION CONVERTER
120
RESOLUTION CONVERTER
122
RESOLUTION CONVERTER
SD10
SD20
SD30
116A
SELECTOR
VS1(D)
VPC(D)
VS2(D)
110
DIGITAL DECODER
112
DIGITAL DECODER
114
DIGITAL DECODER
VPC(A)
VS1(A)
VS2(A)

Fig. 11

Fig. 12(A)

SD1:VPC, SD2:VS1
SD3:VS2

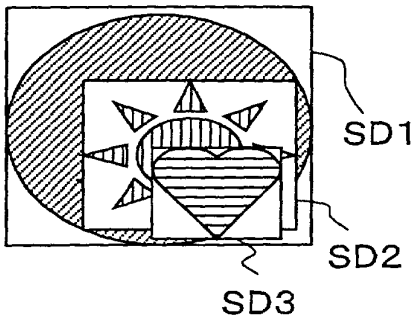


Fig. 12(B)

SD1:VPC, SD2:VS2
SD3:VS1

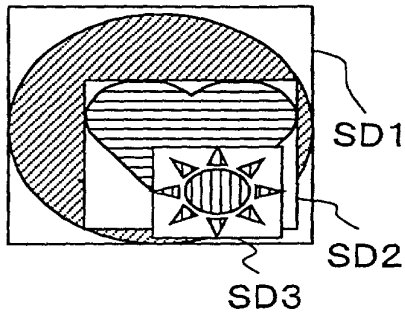


Fig. 12(C)

SD1:VS1, SD2:VS2
SD3:VPC

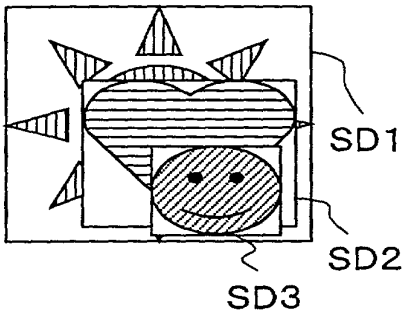


Fig. 12(D)

SD1:VS1, SD2:VPC
SD3:VS2

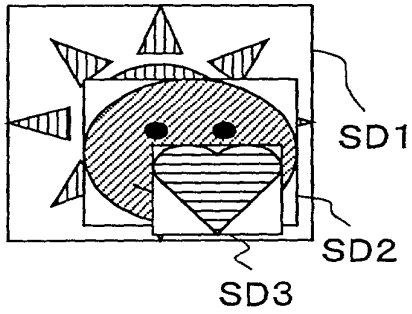


Fig. 12(E)

SD1:VS2, SD2:VS1
SD3:VPC

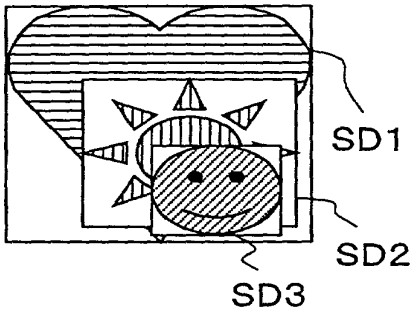
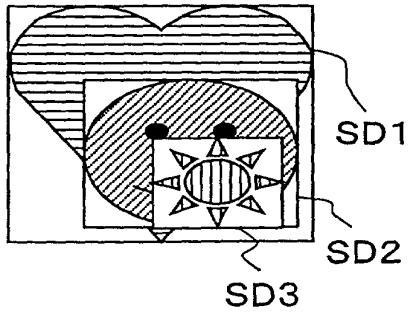


Fig. 12(F)

SD1:VS2, SD2:VPC
SD3:VS1



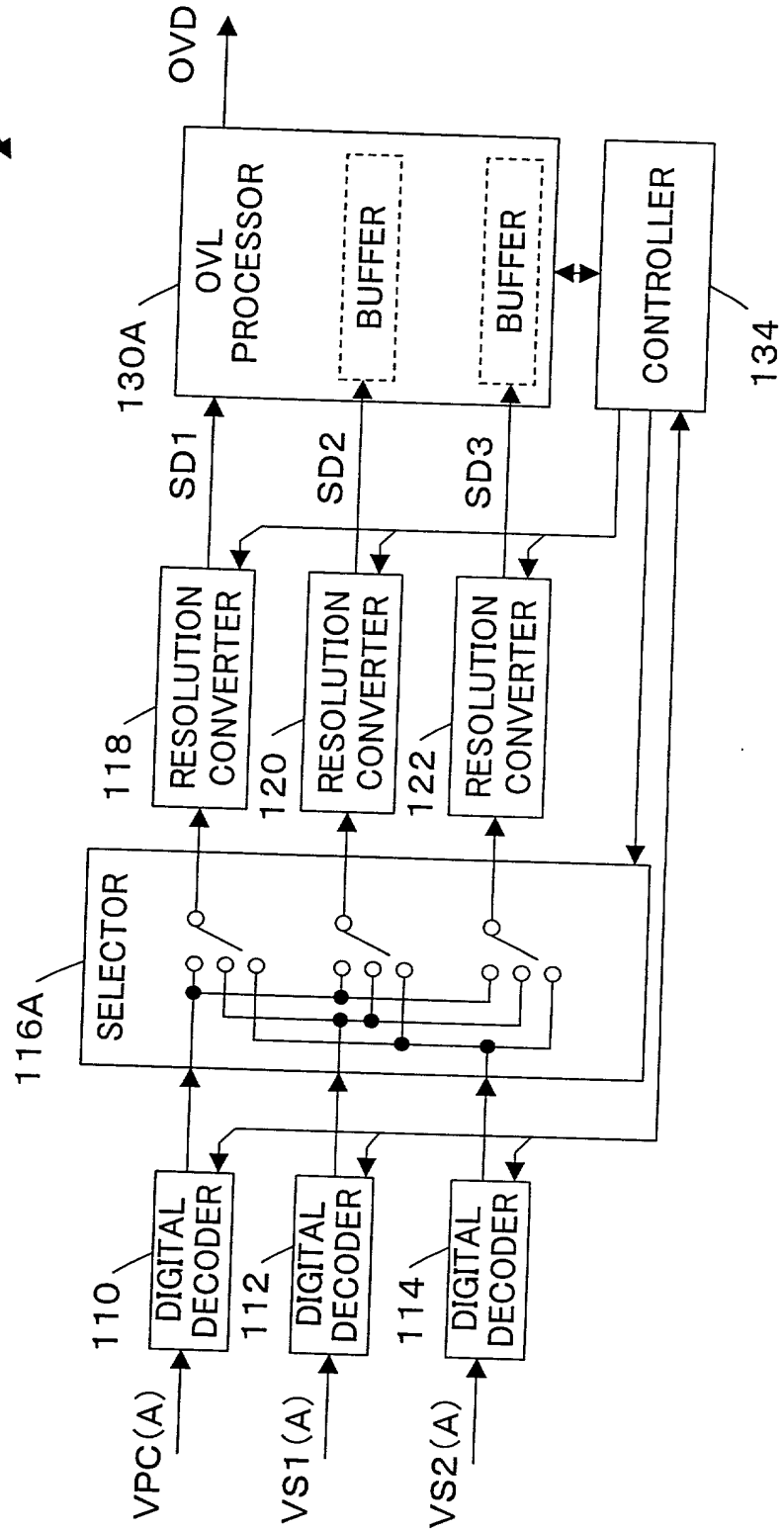

10C
OVD
130A
OVL PROCESSOR
BUFFER
BUFFER
CONTROLLER
134
SD1
SD2
SD3
118
RESOLUTION CONVERTER
120
RESOLUTION CONVERTER
122
RESOLUTION CONVERTER
116A
SELECTOR
110
DIGITAL DECODER
112
DIGITAL DECODER
114
DIGITAL DECODER
VPC(A)
VS1(A)
VS2(A)

Fig. 13